In The Drawings:

Please substitute the attached replacement drawing sheets comprising corrected Figures 1, 2, 4, 5, 6. Figures 1 and 2 have been designated with the legend "Prior Art". Figure 4 has been amended to correct the spelling of "transmit" and the reference numeral 308 has been amended to 380. In Figures 5 and 6, reference numerals have been added to identify the elements therein. Support for this can be found in the specification on page10 beginning at line 13, and page 17 beginning at line 21.

REMARKS

Claims 1-48 are pending and stand rejected. The Examiner's reconsideration of the rejections in view of the above amendments and the following remarks is respectfully requested.

The drawings have been amended to place 'prior art' in Figs. 1 and 2. In Figure 4, "308" is changed to "380" and a signal direction at multiplexer 420 is changed. Numeral labels have been added in Figs. 5 and 6. No new matter is introduced by the changes.

Claims 1, 5-6, 11, 21, 25-26, 35-36, 40, and 44-45 were rejected under 35 U.S.C. §102(b) as anticipated by Funk et al., U.S. Patent 6,026,119. The Examiner stated essentially that Funk teaches all the limitations recited in claims 1, 5-6, 11, 21, 25-26, 35-36, 40, and 44-45, including a "common bus" interconnecting a master controller and plurality of peripherals including a signal modulator/demodulator (modem), the master controller being provided for controlling via the common bus the plurality of peripherals. The Examiner referred to busses "430, 432 and 434" shown in Fig. 4 of Funk as being "the common bus". Claims 1 and 11 have been amended to replace "common bus" with "packet bus".

Applicant respectfully submits that the bus in Funk referred to by the Examiner as "the common bus 430, 432, and 434" and particularly the central processor's bus 432, may be a conventional processor bus, but not a packet bus. A conventional processor bus having A address lines and M data lines, whereas a packet bus has N data lines to carry packetized commands and data, N is less than M. Further, the word "packet" in Funk is used to refer to "wireless packet data communications" and to the operations of the RF

modem 101 configured to receive the "wireless packet data" and not to the packetization of non-wireless data conveyed through the bus 432. See, for example, in Funk column 3, lines 4-7, Funk teaches that "the controller interface (111) is a standard electrical interface, such as the Personal Computer Memory Card International Association (PCMCIA) Card Interface Release 2.0 electrical standard". Thus, the "controller interface (111)" of Funk is NOT a "master controller" having active control functions, thus not controlling the other "peripheral" 425, but rather may be implemented simply as a predetermined ("standard") arrangement of passive "interface" connectors such as pins that function as passive components (conductors) of the bus. Additionally, the "Input/Output (I/O) bus interface (434)" of Funk (Col. 4 line 60) is not the same "bus" as 430 or 432, and thus would not be properly termed a "common" bus.

Claims 1 and 11 each recites, *inter alia*, a plurality of peripherals, "operatively connected to a ... packet bus having N data lines" and "a central processing unit operatively connected to a processor bus including address lines and M data lines, wherein M is greater than N". Claims 1 and 11 further recites "a master controller, operatively connected to the processor bus and to the ... packet bus" "having N data lines", "for controlling via the packet bus [bus having N data lines] a plurality of peripherals operatively connected to [the bus having N data lines]"

Funk discloses a central processor 421 having a processor bus 432, a first peripheral (modem 101) on a second bus 430, and a second peripheral (425) on a third bus 434, the third bus shown as directly connected to the processor, not through any "master controller" 111. Funk does not teach both the first peripheral and the second

peripheral being controlled by a "master controller", nor even being on the same (packet) bus (430), much less "a packet bus" having "N data lines" rather than the M data lines of the processor's bus" as claimed in claims 1 and 11. Therefore, claims 1 and 11 are patentably distinguished and not rendered obvious in view of Funk.

Claims 21 and 31 each recites, *inter alia*, an application processor (AP) comprising: "a processor bus including address lines and M data lines" and "a master controller operatively connected to the processor bus and to a ... bus having N data lines, for controlling via the ... bus the plurality of peripherals, wherein M is greater than N."

Funk does not teach "a ... bus having N data lines" (as distinguished from the M data lines of a processor bus) "for controlling ... the plurality of peripherals" as claimed in claims 21and 31. Nor does Funk disclose "a ... bus having N data lines" (as distinguished from the M data lines of a processor bus) "for controlling ... the plurality of peripherals". Therefore, Funk does not anticipate nor render obvious claims 21 and 31.

Claim 40 recites, *inter alia*, a method comprising: "controlling a master controller via a processor bus", "controlling a plurality of peripherals including the signal modulator/demodulator via a common bus", and "operatively connected to the master controller and to each of the plurality of peripherals."

Funk arguably teaches a second peripheral on a third bus shown as directly connected to the processor, but not through any "master controller" 111. Therefore, Funk does not teach "a common bus" (distinct from the "processor bus") "operatively connected to the master controller and to each of the plurality of peripherals." Further, Funk does not teach both the first peripheral (modem 101) and the second peripheral

(425) being on the same "common bus" (distinct from the processor's bus 432) and being controlled by a "master controller". Thus, Claim 40 is neither disclosed nor suggested by Funk.

Claims 5-6 depend from claim 1. Claims 25-26 depend from claim 21. Claims 35-36 depend from claim 31. Claims 44-45 depend from claim 40. These dependent claims are believed to be allowable for at least the reasons given for claims 1, 11, 21, 31, and 40.

Claims 2-7, 11-12, 14-16, 18, 22-23, 27, 32-33, 37, 41 and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Funk et al., U.S. Patent 6,026,119 in view of Gibbs et al. (US Pat. Appl. # 2003/0114152). Claims 2-10, 12-20, 22-30, 32-39, 41-48 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Funk et al., U.S. Patent 6,026,119 in view of other art (Wilska et al. US Pat Appl# 2002/0082043; Watanabe, US Pat# 6,378,102, Feuki, US Pat Appl# 2002/0166058). However, neither Gibbs nor the other art cited by the Examiner disclose or suggest the bus-related features claimed in the independent claims and which have been shown above to be absent from Funk (U.S. Patent 6,026,119). Thus, the deficiencies in Funk are not cured by Gibbs or the other references. Therefore, each of dependent claims 2-10, 12-20, 22-30, 32-39, 41-48 are believed to be allowable for at least the reasons given for the independent claims 1, 11, 21, and 31, and 40.

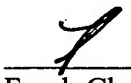
The dependent claims are patentable over the cited references for additional reasons. For example, none of the references disclose "a shared memory operatively connected to the modem and the master controller for access by either the modem or the

central processing unit" as in claim 2. There is no suggestion that the shared memory is an SDRAM, as in claim 3, nor wherein the plurality of peripherals operatively connected to the packet bus includes the modem and at least one of an image capture module, a display, and a flash memory as in claim 4, much less the particularized features of the shared memory or SDRAM, as recited in claims 7 to 10.

The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-48, is believed to be in condition for allowance. Early and favorable action is respectfully urged.

Respectfully submitted,

By: 

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